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RESPONSE TO RESTRICTION REQUIREMENT AND PRELIMINARY AMENDMENT

Sir:

Restriction Requirement. In response to the Examiner's requirement for an election of the claims, mailed February 25, 2003, in the above-identified patent application, Applicant elects Group I, Claims 66-88 and 130-189, and new Claims 190-203, drawn to a semiconductor device.

Preliminary Amendment. Prior to substantive examination, Applicant requests that the following amendments be made to the above-referenced application.

IN THE CLAIMS

Please amend the claims as shown in the attached replacement sheets submitted under 37 C.F.R. § 1.121(c). A blacklined version is enclosed to illustrate the amendments to the claims.

REMARKS

Claims 66-88 and 130-203 are pending. Claims 190-203 have been added. Support for the newly added claims is in the original method claims as filed. No new matter is added.

Claims 1-65 and 89-129 (Group II), drawn to methods, have been cancelled without prejudice to their future prosecution in response to the Examiner's requirement for restriction. Applicant reserves the right to file divisional applications on the non-elected claims.

Applicant believes that the claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

Kristine M. Strodthoff

Dated: March 10, 2003

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WHAT IS CLAIMED IS:

66. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a silicon-comprising ceramic;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

67. The capacitor of Claim 66, wherein the nanostructures comprise a silicon oxycarbide ceramic.

68. The capacitor of Claim 66, wherein the nanostructures are in the form of porous structures.

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69. The capacitor of Claim 66, wherein the nanostructures are in the form of relief structures.

70. The capacitor of Claim 69, wherein the nanostructures are in the form of struts.

71. The capacitor of Claim 66, wherein the nanostructures are formed by ultraviolet irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block.

72. The capacitor of Claim 71, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief nanostructure.

73. The capacitor of Claim 71, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous nanostructure.

74. The capacitor of Claim 71, wherein the hydrocarbon block comprises polyisoprene, and the silicon-comprising block comprises poly(pentamethyldisilylstyrene).

Replacement Claims

75. The capacitor of Claim 71, wherein the polymeric material comprises poly(dimethylsiloxane).

76. The capacitor of Claim 66, wherein the dielectric layer comprises silicon nitride.

77. The capacitor of Claim 66, wherein the upper capacitor electrode comprises a doped polysilicon.

78. The capacitor of Claim 66, wherein the upper capacitor electrode comprises a conductive metal.

79. The capacitor of Claim 66, wherein the capacitor is integrated into a DRAM cell.

80. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a silicon oxycarbide ceramic;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

81. The capacitor of Claim 80, wherein the nanostructures are in the form of porous structures.

82. The capacitor of Claim 80, wherein the nanostructures are in the form of relief structures.

83. The capacitor of Claim 82, wherein the nanostructures are in the form of struts.

84. The capacitor of Claim 83, wherein the nanostructures comprise an ultraviolet irradiated and ozonolyzed polymeric material comprising a hydrocarbon block and a silicon-containing block.

85. The capacitor of Claim 80, wherein the capacitor is integrated into a DRAM cell.

86. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a polymeric silicon-comprising ceramic formed by UV irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

87. The capacitor of Claim 86, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief nanostructure.

88. The capacitor of Claim 86, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous nanostructure.

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130. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising surface dislocations comprising an annealed conductive metal, and the overlying conductive layer comprising clusters of a conductive metal formed on the surface dislocations of the texturizing layer;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

131. The capacitor of Claim 130, wherein the texturizing layer comprises a strain relief pattern.

132. The capacitor of Claim 130, wherein the texturizing layer comprises a trigonal dislocation network comprising a plurality of unit cells.

133. The capacitor of Claim 130, wherein the overlying conductive layer comprises one island cluster within a single unit cell of the dislocation network.

134. The capacitor of Claim 130, wherein the texturizing layer comprises an annealed layer of a first and second conductive metal, the first conductive metal selected from the group consisting of platinum, and the second conductive metal is selected from the group consisting of silver, and copper.

135. The capacitor of Claim 130, wherein the texturizing layer comprises an annealed layer of platinum and silver, and the overlying conductive layer comprises a gaseous deposit of silver.

136. The capacitor of Claim 130, wherein the texturizing layer comprises an annealed layer of platinum and copper, and the overlying conductive layer comprises a gaseous deposit of cobalt.

137. The capacitor of Claim 130, wherein the upper capacitor plate comprises a doped polysilicon.

138. The capacitor of Claim 130, wherein the upper capacitor plate comprises a conductive metal.

139. The capacitor of Claim 130, wherein the capacitor is integrated into a DRAM cell.

140. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising a periodic network of surface dislocations comprising an annealed conductive metal overlying the insulative layer; and the lower capacitor plate comprising an ordered array of nanostructures formed on the surface dislocations of the texturizing layer;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

141. The capacitor of Claim 140, wherein the texturizing layer comprises an annealed layer of a first and second conductive metal, and the overlying conductive layer comprises a gaseous deposit of a third conductive metal.

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142. The capacitor of Claim 140, wherein the texturizing layer comprises platinum and silver, and the overlying conductive layer comprises silver.

143. The capacitor of Claim 140, wherein the texturizing layer comprises platinum and copper, and the overlying conductive layer comprises cobalt.

144. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising an annealed layer of a first and second conductive metal comprising surface dislocations, and the conductive layer comprising agglomerated island clusters of a conductive metal on the surface dislocations of the texturizing layer;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

145. The capacitor of Claim 144, wherein the conductive layer comprises a gaseous deposit of a third conductive metal to form the agglomerated island clusters.

146. The capacitor of Claim 144, wherein the texturizing layer comprises platinum and silver, and the overlying conductive layer comprises silver.

147. The capacitor of Claim 144, wherein the texturizing layer comprises a strain relief pattern.

148. The capacitor of Claim 144, wherein the texturizing layer comprises a trigonal dislocation network comprising a plurality of unit cells.

149. The capacitor of Claim 148, wherein the overlying conductive layer comprises one island cluster within a single network unit cell of the texturizing layer.

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150. The capacitor of Claim 144, wherein the capacitor is integrated into a DRAM cell.

151. A semiconductor circuit, comprising a capacitor;

the capacitor comprising a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a silicon oxycarbide ceramic and formed by ultraviolet irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block.

152. The semiconductor circuit of Claim 151, wherein the nanostructures form a periodic network, and the overlying conductive layer comprises an ordered array of island clusters.

153. The semiconductor circuit of Claim 151, wherein the nanostructures are in the form of porous structures.

154. The semiconductor circuit of Claim 151, wherein the nanostructures are in the form of relief structures.

155. The semiconductor circuit of Claim 151, wherein the conductive layer of the lower capacitor electrode comprises doped amorphous silicon, pseudo-crystalline silicon, or polycrystalline silicon.

156. The semiconductor circuit of Claim 151, wherein the conductive layer of the lower capacitor electrode comprises a conductive metal.

157. A semiconductor circuit, comprising a capacitor;

the capacitor comprising a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising an annealed layer of a first and a second conductive metal comprising surface dislocations; and the overlying conductive layer comprising agglomerated island clusters of a conductive metal on the surface dislocations of the texturizing layer.

158. An integrated circuit, comprising:

an array of memory cells;

internal circuitry; and

at least one capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array, the capacitor comprising a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a polymeric silicon-comprising ceramic formed by UV irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block.

159. An integrated circuit, comprising:

an array of memory cells;

internal circuitry; and

at least one capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array, the capacitor comprising a lower

capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising an annealed layer of a first and a second conductive metal comprising surface dislocations; and the overlying conductive layer comprising agglomerated island clusters of a conductive metal on the surface dislocations of the texturizing layer.

160. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising an ordered array of nanostructures of substantially uniform size;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

161. The capacitor of Claim 160, wherein the texturizing layer comprises a polymeric material.

162. The capacitor of Claim 161, wherein the polymeric material comprises a hydrocarbon block and a silicon-containing block.

163. The capacitor of Claim 162, wherein the polymeric material comprises polyisoprene and poly(pentamethyldisilylstyrene).

164. The capacitor of Claim 160, wherein the texturizing layer comprises a conductive material.

165. The capacitor of Claim 164, wherein the texturizing layer comprises at least two conductive metals.

166. The capacitor of Claim 165, wherein the texturizing layer comprises platinum, and at least one of silver and copper.

167. The capacitor of Claim 164, wherein the conductive layer comprises a plurality of metal island clusters.

168. The capacitor of Claim 160, wherein the texturizing layer comprises a plurality of two-dimensional structures.

169. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising a periodic network of surface structures having a substantially uniform height;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

B2 Cont'D.

170. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising an ordered array of nanostructures of substantially uniform dimensions;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

171. A semiconductor circuit, comprising a capacitor according to Claim 160.

172. The circuit of Claim 171, wherein the texturizing layer comprises a polymeric material.

173. The circuit of Claim 172, wherein the polymeric material comprises a hydrocarbon block and a silicon-containing block.

174. The circuit of Claim 171, wherein the texturizing layer comprises a conductive material.

175. The circuit of Claim 174, wherein the texturizing layer comprises at least two conductive metals.

176. The circuit of Claim 175, wherein the texturizing layer comprises platinum, and at least one of silver and copper.

177. A semiconductor circuit, comprising a capacitor according to Claim 169.

178. A semiconductor circuit, comprising a capacitor according to Claim 170.

179. An integrated circuit, comprising:
an array of memory cells;
internal circuitry; and
at least one capacitor according to Claim 160, the capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array.

180. The circuit of Claim 179, wherein the texturizing layer comprises a polymeric material.

181. The circuit of Claim 180, wherein the polymeric material comprises a hydrocarbon block and a silicon-containing block.

182. The circuit of Claim 179, wherein the texturizing layer comprises a conductive material.

183. The circuit of Claim 182, wherein the texturizing layer comprises at least two conductive metals.

184. The circuit of Claim 183, wherein the texturizing layer comprises platinum, and at least one of silver and copper.

Replacement Claims

185. An integrated circuit, comprising:

an array of memory cells;

internal circuitry; and

at least one capacitor according to Claim 169, the capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array.

186. An integrated circuit, comprising:

an array of memory cells;

internal circuitry; and

at least one capacitor according to Claim 170, the capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array.

187. An integrated circuit supported by a substrate, and comprising a capacitor according to Claim 66.

188. An integrated circuit supported by a substrate, and comprising a capacitor according to Claim 130.

189. An integrated circuit supported by a substrate, and comprising a capacitor according to Claim 160.

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190. (new) A lower capacitor electrode, produced by the process of:

depositing a polymeric material comprising a hydrocarbon block and a silicon-containing block onto an insulative layer; and exposing the polymer material to ozone and electromagnetic radiation to form a texturizing layer comprising an ordered array of nanostructures of substantially uniform size; and

forming a conductive layer over the texturizing layer.

191. (new) The electrode of Claim 190, wherein the polymeric material comprises a triblock copolymer of the type A_1BA_2, where the "A" copolymer is the hydrocarbon block and the "B" copolymer is the silicon-containing block.

192. (new) The electrode of Claim 190, wherein the polymeric material comprises polyisoprene and poly(pentamethyldisilylstyrene).

193. (new) A lower capacitor electrode, produced by the process of:

depositing a first conductive metal onto an insulative layer, depositing a second conductive metal onto the first conductive metal, and annealing the metals to form a texturizing layer; and

B3 cont'd.

forming a conductive layer over the texturizing layer.

194. (new) The electrode of Claim 193, wherein the texturizing layer comprises platinum, and at least one of silver and copper.

195. (new) The electrode of Claim 193, wherein the step of forming the conductive layer over the texturizing layer comprises depositing a conductive metal in a gaseous phase.

196. (new) The electrode of Claim 193, wherein the conductive layer comprises metal island clusters.

197. (new) A lower capacitor electrode, produced by the process of:

depositing a texture-forming material onto an insulating layer;

forming the material into an ordered array of nanostructures of substantially uniform dimensions; and

depositing a conductive layer onto the nanostructures.

Replacement Claims

198. (new) A capacitor, produced by the process of:

depositing a silicon-comprising hydrocarbon polymeric material into an opening in an insulating layer, and exposing the polymeric material to ultraviolet radiation and ozone to form a texturizing layer comprising silicon oxycarbide ceramic nanostructures;

forming a conductive layer over the texturizing layer to form a lower capacitor electrode;

forming a dielectric layer over the lower capacitor electrode; and

forming an upper capacitor electrode over the dielectric layer.

199. (new) A lower capacitor electrode, produced by the process of:

depositing a conformal layer of a first conductive metal onto a substrate, depositing one or more conformal layers of a second conductive metal over the first conductive metal layer, and annealing the first and second conductive metal layers to form a texturizing underlayer; and

depositing a layer of a third conductive metal in gas phase onto the texturizing layer.

200. (new) The electrode of Claim 199, wherein the step of depositing the second conductive metal comprises depositing a plurality of monolayers of the second conductive metal.

201. (new) The electrode of Claim 199, wherein the first and second metal layers are annealed to a temperature of about 800K.

202. (new) The electrode of Claim 199, wherein the step of depositing the third conductive metal comprises depositing the metal by evaporation technique at a temperature of about 100K to about 130K.

203. (new) A capacitor, produced by the process of:

depositing a conformal layer of a first conductive metal into an opening in an insulating layer, depositing a conformal layer of a second conductive metal over the first conductive metal layer, and annealing the first and second conductive metal layers to form a texturizing layer over the insulating layer within the opening;

depositing a layer of a third conductive metal in gas phase onto the texturizing layer to form a lower capacitor electrode, wherein the third conductive layer agglomerates onto the texturizing layer to form nanostructures;

forming a dielectric layer over the lower capacitor electrode; and

forming an upper capacitor electrode

WHAT IS CLAIMED IS:

~~1. A method of forming a lower capacitor electrode, comprising the steps of:~~

~~forming a texturizing layer over an insulative layer, the texturizing layer comprising an ordered array of nanostructures of substantially uniform size; and~~

~~forming a conductive layer over the texturizing layer.~~

~~2. The method of Claim 1, wherein the texturizing layer comprises a polymeric material.~~

~~3. The method of Claim 2, wherein the polymeric material comprises a hydrocarbon block and a silicon-containing block.~~

~~4. The method of Claim 3, wherein the polymeric material comprises polyisoprene and poly(pentamethyldisilylstyrene).~~

~~5. The method of Claim 2, wherein the step of forming the texturizing layer comprising depositing a polymeric material comprising a hydrocarbon block and a silicon-containing block onto the insulative layer; and exposing the polymer material to ozone and electromagnetic radiation.~~

~~6. The method of Claim 1, wherein the texturizing layer comprises a conductive material.~~

~~7. The method of Claim 6, wherein the texturizing layer comprises at least two conductive metals.~~

~~8. The method of Claim 7, wherein the texturizing layer comprises platinum, and at least one of silver and copper.~~

~~9. The method of Claim 7, wherein the step of forming the texturizing layer comprises:~~

~~depositing a first conductive metal onto the insulative layer;~~

~~depositing a second conductive metal onto the first conductive metal; and~~

~~annealing the metals to form a strain relief pattern.~~

~~10. The method of Claim 9, wherein the step of forming the conductive layer over the texturizing layer comprises depositing a conductive metal in a gaseous phase.~~

~~11. The method of Claim 10, wherein the conductive layer comprises a plurality of metal island clusters.~~

~~12. The method of Claim 9, wherein the texturizing layer comprises a plurality of two-dimensional structures.~~

~~13. A method of forming a lower capacitor electrode, comprising the steps of:~~

~~forming a texturizing layer over an insulating layer, the texturizing layer comprising a periodic network of surface structures having a substantially uniform height; and~~

~~forming a conductive layer over the texturizing layer.~~

~~14. A method of forming a lower capacitor electrode, comprising the steps of;~~

~~depositing a texture-forming material onto an insulating layer;~~

~~forming the material into an ordered array of nanostructures of substantially uniform dimensions; and~~

~~depositing a conductive layer onto the nanostructures.~~

~~15. A method of forming a lower capacitor electrode in a container formed within an insulative layer overlying a substrate in a semiconductor device, the method comprising the steps of:~~

~~forming a texturizing underlayer by depositing a polymeric material over the insulative layer, and exposing the polymeric material to ultraviolet radiation and ozone whereby the~~

~~polymeric material forms into nanostructures comprising a silicon-comprising ceramic; the polymeric material comprising a hydrocarbon block and a silicon-containing block; and~~

~~forming a conductive layer over the texturizing layer.~~

~~16. The method of Claim 15, wherein the step of forming the texturizing layer comprises exposing the polymeric material to the ultraviolet light and ozone at room temperature.~~

~~17. The method of Claim 15, wherein the polymeric material comprises a triblock copolymer of the type A_1BA_2, where the "A" copolymer is the hydrocarbon block and the "B" copolymer is the silicon-containing block.~~

~~18. The method of Claim 17, wherein the hydrocarbon block comprises polyisoprene.~~

~~19. The method of Claim 17, wherein the silicon-comprising block comprises poly(pentamethyldisilylstyrene).~~

~~20. The method of Claim 15, wherein the polymeric material comprises poly(dimethylsiloxane).~~

~~21. The method of Claim 15, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief structure.~~

~~22. The method of Claim 15, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous structure.~~

~~23. The method of Claim 15, wherein the step of depositing the polymeric material comprises a vapor deposition polymerization.~~

~~24. The method of Claim 15, wherein the step of depositing the polymeric material comprises field enhanced polymerization vapor deposition polymerization.~~

~~25. The method of Claim 15, wherein the step of depositing the polymeric material comprises a spin-on deposition.~~

~~26. The method of Claim 15, wherein the step of depositing the polymeric material comprises a Langmuir-Blodgett deposition.~~

~~27. The method of Claim 15, wherein the nanostructures are in the form of porous structures.~~

~~28. The method of Claim 15, wherein the nanostructures are in the form of relief structures.~~

~~29. The method of Claim 28, wherein the relief structures are selected from the group consisting of struts and gyroids.~~

~~30. The method of Claim 28, wherein the nanostructures are in the form of struts.~~

~~31. The method of Claim 15, further comprising, after the step of forming the conductive layer, the steps of:~~

~~forming a dielectric layer over the lower electrode; and~~

~~forming an upper capacitor electrode over the dielectric layer.~~

~~32. The method of Claim 15, wherein the substrate comprises a diffusion area, and a conductive plug is formed in an opening through the insulative layer and in electrical contact with the diffusion area and the lower capacitor electrode.~~

~~33. The method of Claim 15, wherein the capacitor is integrated into a DRAM cell.~~

~~34. A method of forming a capacitor in a semiconductor device, comprising the steps of:~~

~~providing a substrate comprising a diffusion area, an insulative layer overlying the substrate, a conductive plug formed in an opening through the insulative layer and in electrical contact with the diffusion area in the substrate, and a container opening formed through the insulating layer to expose a portion of the conductive plug;~~

~~forming a texturizing layer by depositing a silicon-comprising hydrocarbon polymeric material over the insulating layer and the conductive plug, and exposing the polymeric material to ultraviolet radiation and ozone to form nanostructures comprising a silicon oxycarbide ceramic;~~

~~removing at least a portion of the texturizing layer to expose the conductive plug;~~

~~forming a conductive layer over the texturizing layer to form the lower capacitor electrode;~~

~~forming a dielectric layer over the lower electrode; and~~

~~forming an upper capacitor electrode over the dielectric layer.~~

~~35. The method of Claim 34, wherein the polymeric material comprises a triblock copolymer of the type A_1BA_2, where the "A" copolymer is the hydrocarbon block and the "B" copolymer is the silicon-containing block.~~

~~36. The method of Claim 35, wherein the hydrocarbon block comprises polyisoprene.~~

~~37. The method of Claim 35, wherein the silicon-comprising block comprises poly(pentamethyldisilylstyrene).~~

~~38. The method of Claim 34, wherein the polymeric material comprises poly(dimethylsiloxane).~~

~~39. The method of Claim 34, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief structure.~~

~~40. The method of Claim 34, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous structure.~~

~~41. The method of Claim 34, further comprising, after the step of forming the conductive layer, the steps of:~~

~~forming a barrier layer to fill the container;~~

~~removing the conductive layer from horizontal surfaces of the insulative layer; and~~

~~removing the barrier layer from the container.~~

~~42. The method of Claim 41, wherein the barrier layer comprises a resist material.~~

~~43. The method of Claim 41, wherein the step of removing the conductive layer is by chemical-mechanical polishing.~~

~~44. The method of Claim 41, further comprising, after the step of removing the barrier layer, the step of removing native oxide from exposed surfaces of the insulating layer and the conductive layer.~~

~~45. The method of Claim 44, wherein the step of removing the native oxide is by a hydrofluoric acid clean.~~

~~46. A method of forming a capacitor in a semiconductor device, the semiconductor device comprising a substrate having a diffusion area formed therein, an insulative layer overlying the substrate, a conductive plug formed in an opening through the insulative layer and in electrical contact with the diffusion area in the substrate, and a container opening formed through the insulating layer to expose a portion of the conductive plug; the method comprising the steps of:~~

~~forming a texturizing layer over the insulating layer and the conductive plug by depositing a silicon-comprising hydrocarbon polymeric material thereover and exposing the~~

~~polymeric material to ultraviolet radiation and ozone, whereby the polymeric material forms nanostructures comprising a silicon-comprising ceramic;~~

~~removing at least a portion of the texturizing layer to expose the conductive plug;~~

~~forming a conductive layer over the texturizing layer to form the lower capacitor electrode;~~

~~forming a dielectric layer over the lower electrode; and~~

~~forming an upper capacitor electrode over the dielectric layer.~~

~~47. The method of Claim 46, wherein the texturizing layer comprises a silicon oxycarbide ceramic.~~

~~48. The method of Claim 46, wherein the step of forming the texturizing layer comprises exposing the polymeric material to the ultraviolet light and ozone at room temperature.~~

~~49. The method of Claim 46, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief structure.~~

~~50. The method of Claim 46, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous structure.~~

~~51. The method of Claim 46, wherein the nanostructures are in the form of struts.~~

~~52. A method of forming a lower capacitor electrode in a semiconductor device, the semiconductor device comprising a substrate, an insulative layer overlying the substrate, a conductive plug formed within an opening in the insulative layer and in electrical contact with an active area within the substrate, and an opening formed through the insulating layer and exposing a surface of the conductive plug; the method comprising the steps of:~~

~~forming a texturizing layer comprising nanostructures comprising a silicon- comprising ceramic, the texturizing layer formed by depositing a polymeric material over the insulating layer~~

~~and the conductive plug, and exposing the polymeric material to ultraviolet radiation and ozone at room temperature to form the nanostructures; the polymeric material comprising a hydrocarbon block and a silicon-containing block;~~

~~removing at least a portion of the texturizing layer to expose the conductive plug; and~~

~~forming a conductive layer over the texturizing layer to form the lower capacitor electrode.~~

~~53. The method of Claim 52, wherein the nanostructures comprise a silicon oxycarbide ceramic.~~

~~54. The method of Claim 52, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief structure.~~

~~55. The method of Claim 52, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous structure.~~

~~56. The method of Claim 52, wherein the polymeric material comprises a triblock copolymer of the type A_1BA_2, where the "A" copolymer is the hydrocarbon block and the "B" copolymer is the silicon-containing block.~~

~~57. The method of Claim 56, wherein the hydrocarbon block comprises polyisoprene, and the silicon-comprising block comprises poly(pentamethyldisilylstyrene).~~

~~58. The method of Claim 52, wherein the polymeric material comprises poly(dimethylsiloxane).~~

~~59. A method of forming a capacitor in a semiconductor device, the semiconductor device comprising a substrate, an insulative layer overlying the substrate, a conductive plug formed within an opening in the insulative layer and in electrical contact with an active area within the~~

~~substrate, and a container formed through the insulating layer and exposing a surface of the conductive plug; the method comprising the steps of:~~

~~forming a texturizing layer comprising nanostructures comprising a silicon-comprising ceramic, the texturizing layer formed by depositing a polymeric material over the insulating layer and the conductive plug, and exposing the polymeric material to ultraviolet radiation and ozone at room temperature to form the nanostructures; the polymeric material comprising a hydrocarbon block and a silicon-containing block;~~

~~removing at least a portion of the texturizing layer to expose the conductive plug; and~~

~~forming a conductive layer over the texturizing layer to form the lower capacitor electrode;~~

~~forming a barrier layer to fill the container;~~

~~removing the conductive layer from horizontal surfaces of the insulative layer;~~

~~removing the barrier layer from the container;~~

~~forming a dielectric layer over the lower electrode; and~~

~~forming an upper capacitor electrode over the dielectric layer.~~

~~60. The method of Claim 59, wherein the nanostructures comprise a silicon oxycarbide ceramic.~~

~~61. The method of Claim 59, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief structure.~~

~~62. The method of Claim 59, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous structure.~~

~~63. The method of Claim 59, wherein the barrier layer comprises a resist material, and the step of removing the barrier layer is by a piranha wet etch comprising sulfuric acid and an oxidant.~~

~~64. The method of Claim 59, wherein the barrier layer is a resist material, and the step of removing the barrier layer is by a wet etch comprising an organic solvent.~~

~~65. The method of Claim 59, further comprising, after the step of removing the barrier layer, the step of removing native oxide from exposed surfaces of the insulating layer and the conductive layer.~~

66. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a silicon-comprising ceramic;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

67. The capacitor of Claim 66, wherein the nanostructures comprise a silicon oxycarbide ceramic.

68. The capacitor of Claim 66, wherein the nanostructures are in the form of porous structures.

69. The capacitor of Claim 66, wherein the nanostructures are in the form of relief structures.

70. The capacitor of Claim 69, wherein the nanostructures are in the form of struts.

71. The capacitor of Claim 66, wherein the nanostructures are formed by ultraviolet irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block.

72. The capacitor of Claim 71, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief nanostructure.

73. The capacitor of Claim 71, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous nanostructure.

74. The capacitor of Claim 71, wherein the hydrocarbon block comprises polyisoprene, and the silicon-comprising block comprises poly(pentamethyldisilylstyrene).

75. The capacitor of Claim 71, wherein the polymeric material comprises poly(dimethylsiloxane).

76. The capacitor of Claim 66, wherein the dielectric layer comprises silicon nitride.

77. The capacitor of Claim 66, wherein the upper capacitor electrode comprises a doped polysilicon.

78. The capacitor of Claim 66, wherein the upper capacitor electrode comprises a conductive metal.

79. The capacitor of Claim 66, wherein the capacitor is integrated into a DRAM cell.

80. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a silicon oxycarbide ceramic;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

81. The capacitor of Claim 80, wherein the nanostructures are in the form of porous structures.

82. The capacitor of Claim 80, wherein the nanostructures are in the form of relief structures.

83. The capacitor of Claim 82, wherein the nanostructures are in the form of struts.

84. The capacitor of Claim 83, wherein the nanostructures comprise an ultraviolet irradiated and ozonolyzed polymeric material comprising a hydrocarbon block and a silicon-containing block.

85. The capacitor of Claim 80, wherein the capacitor is integrated into a DRAM cell.

86. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a polymeric silicon-comprising ceramic formed by UV irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

87. The capacitor of Claim 86, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a relief nanostructure.

88. The capacitor of Claim 86, wherein the polymeric material comprises a volume fraction of the hydrocarbon block relative to the silicon-containing block to form a porous nanostructure.

~~89. A method of forming a lower capacitor electrode over a substrate in a semiconductor device, the method comprising the steps of:~~

~~forming a texturizing underlayer by:~~

~~depositing a conformal layer of a first conductive metal onto the substrate;~~

~~depositing one or more conformal layers of a second conductive metal over the first conductive metal layer;~~

~~annealing the first and second conductive metal layers; and~~

~~depositing a layer of a third conductive metal in gas phase onto the texturizing layer.~~

~~90. The method of Claim 89, wherein the depositing third conductive layer agglomerates into clusters onto the texturizing layer.~~

~~91. The method of Claim 90, wherein the texturizing layer comprises a strain relief pattern.~~

~~92. The method of Claim 89, wherein the step of depositing the first conductive metal is by chemical vapor deposition, or physical vapor deposition.~~

~~93. The method of Claim 89, wherein the step of depositing the second conductive metal is by chemical vapor deposition, evaporation, or physical vapor deposition.~~

~~94. The method of Claim 89, wherein the step of depositing the second conductive metal comprises depositing a plurality of monolayers of the second conductive metal.~~

~~95. The method of Claim 89, wherein the third conductive metal is deposited by an evaporation technique.~~

~~96. The method of Claim 89, wherein the first conductive metal comprises platinum.~~

~~97. The method of Claim 96, wherein the second conductive metal is selected from the group consisting of silver and copper.~~

~~98. The method of Claim 89, wherein the second and third conductive metals comprise silver.~~

~~99. The method of Claim 98, wherein the first and second metal layers are annealed to a temperature of about 800K.~~

~~100. The method of Claim 98, wherein the step of depositing the third conductive metal comprises depositing the silver in gaseous form by evaporation technique at a temperature of about 100K to about 130K.~~

~~101. The method of Claim 89, wherein the first conductive metal is platinum, the second conductive metal is copper, and the third conductive metal is cobalt.~~

~~102. The method of Claim 89, further comprising, after the step of depositing the layer of the third conductive metal, the steps of:~~

~~forming a dielectric layer over the lower capacitor electrode; and~~

~~forming an upper capacitor electrode over the dielectric layer.~~

~~103. The method of Claim 89, wherein the substrate comprises a diffusion area, and a conductive plug is formed in an opening through the insulative layer and in electrical contact with the diffusion area and the lower capacitor electrode.~~

~~104. The method of Claim 89, wherein the capacitor is integrated into a DRAM cell.~~

~~105. A method of forming a lower capacitor electrode in a semiconductor device, the method comprising the steps of:~~

~~forming a texturizing underlayer by depositing a layer of a first conductive metal onto a substrate, and a layer of a second conductive metal over the first conductive metal layer; and annealing the first and second conductive metal layers to form a periodic network of metal-comprising nanostructures; and~~

~~depositing a layer of a third conductive metal in gas phase onto the texturizing layer.~~

~~106. The method of Claim 105, wherein depositing the third conductive metal results in a plurality of island clusters formed over the texturizing layer.~~

~~107. A method of forming a lower capacitor electrode in a container formed within an insulative layer overlying a substrate in a semiconductor device, the method comprising the steps of:~~

~~depositing a layer of a first conductive metal onto the insulative layer;~~

~~depositing a layer of a second conductive metal onto the first conductive metal layer;~~

~~annealing the first and second conductive metal layers to form a texturizing layer comprising periodically arrayed nanostructures; and~~

~~depositing a layer of a third conductive metal in gas phase onto the texturizing layer, wherein the depositing third conductive layer agglomerates onto the texturizing layer to form clusters.~~

~~108. The method of Claim 107, wherein the step of depositing the second conductive metal comprises depositing a plurality of monolayers of the second conductive metal.~~

~~109. The method of Claim 107, wherein the first conductive metal comprises platinum.~~

~~110. The method of Claim 109, wherein the second and third conductive metals comprise silver.~~

~~111. The method of Claim 110, wherein the first and second metal layers are annealed to a temperature of about 800K.~~

~~112. The method of Claim 110, wherein the step of depositing the gas phase third conductive metal is at a temperature of about 100K to about 130K.~~

~~113. The method of Claim 107, wherein the first conductive metal comprises platinum, the second conductive metal comprises copper, and the third conductive metal comprises cobalt.~~

~~114. The method of Claim 107, further comprising, after the step of depositing the layer of the third conductive metal, the steps of:~~

~~forming a dielectric layer over the lower capacitor electrode; and~~

~~forming an upper capacitor electrode over the dielectric layer.~~

~~115. A method of forming a capacitor in a semiconductor device, comprising the steps of:~~

~~providing a substrate comprising a diffusion area, an insulative layer overlying the substrate, a conductive plug formed in an opening through the insulative layer and in electrical contact with the diffusion area in the substrate, and a container opening formed through the insulating layer to expose a portion of the conductive plug;~~

~~forming a texturizing underlayer by:~~

~~depositing a conformal layer of a first conductive metal onto the insulative layer;~~

~~depositing a conformal layer of a second conductive metal over the first conductive metal layer; and~~

~~annealing the first and second conductive metal layers to form metal-comprising surface dislocations over the insulative layer;~~

~~depositing a layer of a third conductive metal in gas phase onto the texturizing layer to form the lower capacitor electrode, wherein the depositing third conductive layer agglomerates onto the surface dislocations of the texturizing layer to form nanostructures;~~

~~forming a dielectric layer over the lower capacitor electrode; and~~

~~forming an upper capacitor electrode over the dielectric layer.~~

~~116. The method of Claim 115, wherein the nanostructures are in the form of island clusters.~~

~~117. The method of Claim 115, wherein the first conductive metal comprises platinum, and the second and third conductive metals comprise silver.~~

~~118. The method of Claim 115, wherein the first conductive metal comprises platinum, the second conductive metal comprises copper, and the third conductive metal comprises cobalt.~~

~~119. The method of Claim 115, further comprising, after the step of depositing the third conductive layer, the steps of forming a barrier layer to fill the container, removing the conductive layers of the lower capacitor electrode from horizontal surfaces of the insulative layer, and removing the barrier layer from the container.~~

~~120. The method of Claim 119, wherein the barrier layer comprises a resist material.~~

~~121. The method of Claim 120, wherein the step of removing the barrier layer comprises a wet etch process.~~

~~122. The method of Claim 119, wherein the step of removing the conductive layers is by chemical-mechanical polishing.~~

~~123. The method of Claim 119, further comprising, after the step of removing the barrier layer, the step of removing native oxide from exposed surfaces of the insulating layer and the lower capacitor electrode.~~

~~124. The method of Claim 123, wherein the step of removing the native oxide comprises a hydrofluoric acid clean.~~

~~125. A method of forming a capacitor in a semiconductor device, the semiconductor device comprising a substrate, an insulative layer overlying the substrate, a conductive plug formed within an opening in the insulative layer and in electrical contact with an active area within the substrate, and a container formed through the insulating layer and exposing a surface of the conductive plug; the method comprising the steps of:~~

~~forming a texturizing underlayer by forming a layer of a first conductive metal onto the insulative layer, and a layer of a second conductive metal over the first conductive metal layer; and annealing the first and second conductive metal layers to form metal-comprising surface dislocations over the insulative layer; and~~

~~forming a conductive layer over the texturizing layer to form the lower capacitor electrode by depositing a layer of a third conductive metal in gas phase onto the texturizing layer, wherein the depositing third conductive layer agglomerates onto the texturizing layer to form island clusters on the surface dislocations of the texturizing layer;~~

~~forming a barrier layer to fill the container;~~

~~removing the conductive layers from horizontal surfaces of the insulative layer;~~

~~removing the barrier layer from the container;~~

~~forming a dielectric layer over the lower electrode; and~~

~~forming an upper capacitor electrode over the dielectric layer.~~

~~126. The method of Claim 125, wherein the third conductive metal is deposited in gaseous form by an evaporation technique.~~

~~127. The method of Claim 125, wherein the first conductive metal comprises platinum.~~

~~128. The method of Claim 127, wherein the second and third conductive metals comprise silver.~~

~~129. The method of Claim 125, further comprising, after the step of removing the barrier layer, the step of removing native oxide from exposed surfaces of the insulating layer and the conductive layer.~~

130. A capacitor, comprising:

a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising surface dislocations comprising an annealed conductive metal, and

the overlying conductive layer comprising clusters of a conductive metal formed on the surface dislocations of the texturizing layer;

a dielectric layer overlying the lower capacitor plate; and

an upper capacitor plate overlying the dielectric layer.

131. The capacitor of Claim 130, wherein the texturizing layer comprises a strain relief pattern.

132. The capacitor of Claim 130, wherein the texturizing layer comprises a trigonal dislocation network comprising a plurality of unit cells.

133. The capacitor of Claim 130, wherein the overlying conductive layer comprises one island cluster within a single unit cell of the dislocation network.

134. The capacitor of Claim 130, wherein the texturizing layer comprises an annealed layer of a first and second conductive metal, the first conductive metal selected from the group consisting of platinum, and the second conductive metal is selected from the group consisting of silver, and copper.

135. The capacitor of Claim 130, wherein the texturizing layer comprises an annealed layer of platinum and silver, and the overlying conductive layer comprises a gaseous deposit of silver.

136. The capacitor of Claim 130, wherein the texturizing layer comprises an annealed layer of platinum and copper, and the overlying conductive layer comprises a gaseous deposit of cobalt.

137. The capacitor of Claim 130, wherein the upper capacitor plate comprises a doped polysilicon.

an upper capacitor plate overlying the dielectric layer.

145. The capacitor of Claim 144, wherein the conductive layer comprises a gaseous deposit of a third conductive metal to form the agglomerated island clusters.

146. The capacitor of Claim 144, wherein the texturizing layer comprises platinum and silver, and the overlying conductive layer comprises silver.

147. The capacitor of Claim 144, wherein the texturizing layer comprises a strain relief pattern.

148. The capacitor of Claim 144, wherein the texturizing layer comprises a trigonal dislocation network comprising a plurality of unit cells.

149. The capacitor of Claim 148, wherein the overlying conductive layer comprises one island cluster within a single network unit cell of the texturizing layer.

150. The capacitor of Claim 144, wherein the capacitor is integrated into a DRAM cell.

151. A semiconductor circuit, comprising a capacitor;

the capacitor comprising a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a silicon oxycarbide ceramic and formed by ultraviolet irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block.

152. The semiconductor circuit of Claim 151, wherein the nanostructures form a periodic network, and the overlying conductive layer comprises an ordered array of island clusters.

153. The semiconductor circuit of Claim 151, wherein the nanostructures are in the form of porous structures.

154. The semiconductor circuit of Claim 151, wherein the nanostructures are in the form of relief structures.

155. The semiconductor circuit of Claim 151, wherein the conductive layer of the lower capacitor electrode comprises doped amorphous silicon, pseudo-crystalline silicon, or polycrystalline silicon.

156. The semiconductor circuit of Claim 151, wherein the conductive layer of the lower capacitor electrode comprises a conductive metal.

157. A semiconductor circuit, comprising a capacitor;

the capacitor comprising a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising an annealed layer of a first and a second conductive metal comprising surface dislocations; and the overlying conductive layer comprising agglomerated island clusters of a conductive metal on the surface dislocations of the texturizing layer.

158. An integrated circuit, comprising:

an array of memory cells;

internal circuitry; and

at least one capacitor formed in a container and in electrical contact with an active area within a semiconductive substrate of the memory cell array, the capacitor comprising a lower capacitor plate comprising a conductive layer overlying a texturizing layer; the texturizing layer comprising nanostructures comprising a polymeric silicon-comprising ceramic formed by UV irradiation and ozonolysis of a polymeric material comprising a hydrocarbon block and a silicon-containing block.